REMARKS/ARGUMENTS

Favorable reconsideration of this application, as presently amended and in light of the following discussion is respectfully requested.

Claims 2-6 are pending in the application; Claims 2 and 6 are amended by the present amendment. No new matter is added.

In the outstanding Office Action, Claim 6 was objected to as including informalities; Claims 2, 3 and 6 were rejected under 35 U.S.C. §103(a) as obvious over Debling (U.S. Pat. No. 6,973,592); Claim 4 was rejected under 35 U.S.C. 103(a) as unpatentable over Debling in view of Miura (U.S. Pat. No. 6,918,058); and Claim 5 was rejected under 35 U.S.C. as unpatentable over Debling in view of Windows 2000 Device Driver Book (herein, "Win2k").

With respect the objection to Claim 6, Claim 6 has been amended to recite "on the basis of a select signal input to a given terminal from an external source." Accordingly, Applicants respectfully request that the objection to Claim 6 be withdrawn.

Addressing now the rejection of Claims 2, 3 and 6 based on Debling, that rejection is traversed by the present response.

Claim 2 recites, in part,

> said plurality of processors comprise first and second processors,
> said plurality of debug executing units comprises a first debug executing unit connected to said first processor and a second debug executing unit connected to said second processor,
> said plurality of controllers comprises a first controller connected to said first debug executing unit and a second controller connected to said second debug executing unit,
> said selecting circuit is connected between said first and second controllers and said set of terminals, and
> said selecting circuit inputs, to one or both of said first and second controllers, a debugging signal that is provided commonly from said debugging device through said set of terminals.

Debling describes an on-chip emulator 120 which is connected to a microprocessor 110 and a USB interface 140. In a multi-chip system several USB interfaces 140 are connected to a single USB hub 170 which directs traffic from the several USB interfaces 140. In addition, the USB hub 170 is connected to a universal serial bus 152 which connects the circuit chip to a host device external to the circuit chip, for example, a debugging computer having a USB port.[1] Further, the host device includes a proxy server which connects a program running on the host with a device or service with the required device or service of the target device.

However, Debling does not describe or suggest that the selecting circuit is connected ***between said first and second controllers and said set of terminals***. In addition, Debling does not describe or suggest that the selecting circuit inputs, to one or both of said first and second controllers, ***a debugging signal that is provided commonly from said debugging device through said set of terminals***.

The outstanding Action states on page 2 in the section entitled response to arguments that "[t]he previous rejection erroneously cited a USB hub as such a selecting circuit...[t]he examiner concedes that a USB hub generally only provides a connection as argued by the Applicant. In the system taught by Debling ('592)...[a] host controls the debugging through the USB port. Debling ('592) describes the use of a host proxy server to perform USB functions on behalf of the host. In order to target a specific processor...the host proxy server must add USB address information to a debug command...[t]he USB device address embedded in the USB signal allows the host proxy server to select which specific USB device...will execute a command." In addition, the outstanding Action states on page 4 that "the proxy server exists between the host and the USB interface of each target processor."

[1] Debling, col. 3, lines 50-54.

However, Claim 2 recites that the selecting circuit (which the outstanding Action has equated with the proxy server) is connected ***between said first and second controllers and said set of terminals***. As is illustrated in a non-limiting example in Figure 1 of the present disclosure, the "set of terminals" (2-6) are on the right side of the "selecting circuit" (10) and the first and second "tap controllers" (9_0 and 9_1) are on the left side of the "selecting circuit" (10) therefore clearly the "selecting circuit" (10) is connected ***between said first and second controllers and said set of terminals.*** In contrast, the proxy server of Debling exists between the host (external to the circuit chip) and the input on the USB hub 170.[2] Thus, the proxy server of Debling cannot possibly be equivalent to the selecting circuit recited in Claim 2.

In addition, Debling does not describe or suggest that the selecting circuit inputs, to one or both of said first and second controllers, ***a debugging signal that is provided commonly from said debugging device through said set of terminals***.

As acknowledged by the outstanding Action, Debling describes that each debug command includes an USB address directing the command to a specific processor, in contrast, Claim 1 recites that the debugging signal is commonly provided to both the first and second controllers. Thus, in the situation where both processors need to be debugged the claimed invention need only sent a common debugging signal. In contrast, Debling would require individual debugging instructions be sent for each processor.

Therefore Applicants respectfully submit that Claim 2 and claims depending therefrom patentably distinguish over Debling.

Further, with respect to Claim 3, Applicants respectfully traverse the rejection of this Claim under §103(a) as unpatentable over Debling.

Claim 3 recites, in part,

> said plurality of processors comprise first and second processors,

[2] Debling, col. 4, lines 3-4 and Figure 2.

> said debug executing unit comprises a first debug executing unit connected to said first processor and a second debug executing unit connected to said second processor,
> said selecting circuit is connected between said first and second debug executing units and said controller,
> said controller is connected to said set of terminals, and
> said selecting circuit inputs, to one or both of said first and second debug executing units, a debugging signal outputted from said controller.

The outstanding Action relies on Debling as describing the features recited in Claim 3. However, Debling does not describe or suggest a selecting circuit that is connected between said first and second debug executing units and said controller. In a non-limiting example illustrated in Figure 3, it clearly shown that the "debug executing units" (8_0 and 8_1) are on the left side of the "selecting circuit" (30) and the "tap controller" (9) is on the right side of the "selecting circuit". The outstanding Action states that the proxy server of Debling is equivalent to the "selecting circuit". However, the proxy server is clearly not between the controller and the debug executing units. Therefore Applicants respectfully submit that Claim 3 patentably distinguishes over Debling.

Further, with respect to Claim 4, Applicants respectfully traverse the rejection of this Claim under §103(a) as unpatentable over Debling and Miura.

Claim 4 recites, in part,

> said plurality of processors comprise first and second processors,
> said selecting circuit is connected between said first and second processors and said debug executing unit,
> said debug executing unit is connected to said controller,
> said controller is connected to said set of terminals, and
> said selecting circuit inputs, to one or both of said first and second processors, a debugging signal outputted from said debug executing unit.

The outstanding Action acknowledges that Debling does not describe that the selecting circuit inputs, to one or both of said first and second processors, a debugging signal outputted from said debug executing unit. However, Debling also does not describe that the

selecting circuit is connected between said first and second processors and said debug executing unit. As is illustrated in a non-limiting example shown in Figure 4 the selecting circuit (40) is between the Processors (7_0 and 7_1) and the debug executing unit (8). Debling clearly does not describe this configuration.

However, the outstanding Office Action relies on Miura as curing the deficiencies of Debling with respect to Claim 4.

Miura describes a debugging module that is connected to both a first and second microprocessor. However, there is no description or suggestion in Mirura that the debuggin signal is output from a debug executing unit which is connected to a controller, the controller connected to the input terminals. Clearly Mirua does not cure the above noted deficiencies of Debling with respect to Claim 4.

Accordingly, Applicants respectfully submit that Claim 4 patentably distinguishes over Debling and Mirua considered individually or in combination.

Further, the selection circuit recited in the independent claims allows the sharing of terminals, controllers or debug executing units. This enables the control of the debugging process to be facilitated and the size of the debugging circuit to be reduced. In contrast, in Debling the external connection is through the USB interface instead of a JTAG interface, the use of the USB is merely for obtaining an easier external connection. Nowhere does Debling disclose the advantageous features recited in the present invention. Further, the references description of USB technology merely describe a system that facilitates the connection between the host and the device using a hot-plug or the like, the features of control facilitation and reduction in circuit size are not achieve with the device of Debling.

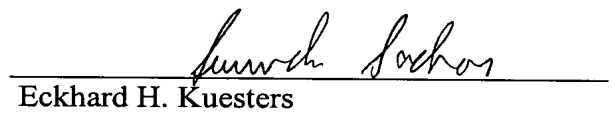
In addition, Applicants respectfully traverse the finality of the rejection given in the outstanding Office Action. MPEP §706.07(a) states "[u]nder present practice, second or any subsequent actions on the merits shall be final, ***except where the examiner introduces a new***

ground of rejection that is neither necessitated by applicant's amendment of the claims nor based on information submitted in an information disclosure statement" (emphasis added). The outstanding Action acknowledges on page 2 that "the previous rejection erroneously cited a USB hub as such a selecting circuit..." Additionally, the outstanding Action now cites the "proxy server" as describing the selecting circuit. Therefore as it is clear that the outstanding Action has introduced a new ground of rejection that is not necessitated by an Amendment or an IDS, Applicants respectfully request that the finality of the Office Action be withdrawn.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



Eckhard H. Kuesters
Attorney of Record
Registration No. 28,870

Surinder Sachar
Registration No. 34,423

Customer Number
22850

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 06/04)

I:\ATTY\JL\242358US\242358US_AM(5.1.2007).DOC